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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,412	11/16/2001	Nigel G. Herron	X-916 US	3726

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,412	HERRON ET AL.	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/13/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21,32 and 33* is/are allowed.

6)☒ Claim(s) *1-18 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicants Amendment filed on 12/13/2004 has been entered and reviewed.

2. Applicant's arguments with respect to claims 1-18 and 22-31 have been considered but are moot in view of the new ground(s) of rejection.

3. The indicated allowability of claims 1-7, 16-18 and 22-31 are withdrawn in view of the newly discovered reference(s) to Shen et al., patent no. 6,829,751.

4. Claims 1-33 are presented for examination.

Claim Rejections - 35 USC ' 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over **Shen et al.** (Shen) patent no. **6,829,751**.

7. As to claim 1, Shen teaches the invention substantially as claimed, including a method for testing a fixed logic device [module 202a of Fig. 5] formed within a gasket [see interface of claim 1] comprising receiving an FPGA scan chain and configuring an FPGA fabric portion for a specified test [col. 4 lines 35-58]; producing a test signal to

the fixed logic device [col. 4 lines 35-58];receiving an output test signal from the fixed logic device [col. 6 lines 57-65].

Shen does not explicitly teach applying a signature function to the received output test signal, repeating the producing, receiving and applying steps for a specified number of times; and determining if a value of the signature function corresponds to an expected value. However, Shen teaches Computer Aided Design (CAD) software may need to be developed for debugging workstation 104 [see Fig. 2] to work together with the on-chip FPGA core 116 by a debugging engineer because of the programming of the FPGA core 116 and the debugging software [see col. 5 lines 13-58 and col. 6 lines 1-30].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to enhance the teachings of Shen by applying a test sequence such as applying a signature function to the received output test signal, repeating the producing, receiving and applying steps for a specified number of times and determining if a value of the signature function corresponds to an expected value for testing a fixed logic device because these test sequence are well known in the art of simulation and testing a logic device and any test engineer is able to write a test program including those test sequence. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a test sequence for testing a logic device.

8. As to claim 2, Shen teaches isolating the fixed logic device [col. 6 lines 45-57].

9. As to claims 3, and 4, Shen teaches transmitting/receiving a test signal to the fixed logic device by way of an isolation circuit element [debugging/bug fix circuit of claim1].

10. As to claim 5, Shen teaches determining step is performed by logic within an FPGA fabric portion [[see claim 1].

11. As to claim 6, Shen teaches determining step is performed by logic an external tester [col. 5 lines 46-53].

12. As to claim 7, Shen teaches determining step includes the step of comparing the signature to an expected value [col. 6 lines 1-30].

13. Claims 8-18 and 22-31 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by **Beebe et al.** (Beebe) patent no. **6,021,513** in view of **Shen et al.** (Shen) patent no. **6,829,751**.

14. As to claim 8, Beebe teaches the invention substantially as claimed, including an FPGA comprising an FPGA fabric portion [see Fig. 9 and claim 6]; a gasket [programmable interconnects, see claim 6] formed at least partially within the FPGA fabric portion, the gasket forming interfacing logic between a programmable logic units and the fabric portion; and isolation circuitry [see claims 8-10] formed within the Gasket, the isolation circuitry being serially coupled to receive test signals from the FPGA portion [see claim 18].

Beebe does not teaches an embedded core device.

Shen teaches a diagnostic architecture using FPGA core in system on a chip design including configuring the FPGA [FPGA core 116 of Fig. Of Fig. 2] for testing a an embedded module [specific module, col. 6 lines 45-57].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Beebe with the teachings of Shen to configure the FPGA scan chain as taught by Beebe for testing the embedded module in a SOC as taught by Shen. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a diagnostic architecture using an FPGA core in a system on a chip (SOC) design [see Shen col. 1 lines 5-11].

15. As to claims 9 and 10, Shen teaches the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signal directly to a device under test [col. 4 lines 12-24 and Fig. 3].

16. As to claim 11, it is similar to claim 8 above, therefore it is rejected under the same rationale. Furthermore, Shen also teaches the FPGA also includes a MUX [MUX 134 of Fig. 2].

17. As to claim 12-15, Shen teaches the MUX 134 is coupled to receive signal from the FPGA 116 to the fixed logic device 130 [see Fig. 2].

18. As to claim 16, it is similar to claim 8 above, therefore it is rejected under the same rationale. Furthermore, Shen teaches an array of isolation circuit elements [debugging/bug fix circuit of claim 1 and scan chain on col. 4 lines 12-24 and Fig. 3].

19. As to claims 17 and 18, Shen teaches the array couple to receive outputs from the embedded device to the FPGA [col. 4 line 59 – col. 5 line 4].

20. As to claim 22, Beebe and Shen teach the invention substantially as claimed including the circuitry for performing the testing and diagnostic function [see claim 1 and Fig. 3]; however, they do not teach the first, second third and fourth logic circuitries as set forth in the instant claim. Official Notice is taken that these circuitries is well known in the art applying for Built-in Self-test (BIST) circuitries.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to realize the combination teachings of Beebe and Shen into hardware by combining the teachings of Beebe and Shen with the circuitries had been well known in the BIST technique for performing the simulation, testing and

diagnostic functions. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a chip with simple BIST circuitries.

21. As to claims 23-24, Shen teaches the logic circuitry is formed communication with a fixed logic device within the gasket col. 4 line 59 – col. 5 line 5].

1. As to claim 25, an embedded core processor is well known. It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to substitute the specific module taught by Shen by an embedded core processor. It is just a matter of application.

22. As to claim 26, it is similar to claim 8 above, therefore it is rejected under the same rationale. Furthermore, Shen teaches a first communication path [I/O port 132 to MUX 143 of Fig. 2] in the gasket that directly coupled at lest a pin of the embedded device to the FPGA fabric portion and a second communication path [combinational logic 130 to MUX 134 of Fig. 2] in the gasket that directly couples the FPGA fabric portion to test circuitry formed within the gasket, which test circuitry further is coupled to at least one pin of the embedded device [see I/O_PIN 150 of Fig. 2].

23. As to claims 27-28, Shen teaches the test circuitry coupled to the FPGA to the embedded device whenever the FPGA configured to test the embedded device [see "interconnecting" of claim 2] and scan chain to the embedded device [col. 6 lines 45-57].

24. As to claim 29, it is similar to claim 8 above, therefore it is rejected under the same rationale. Furthermore, Shen teaches a first communication path coupled the FPGA to test circuitry [I/O port 132 to MUX 143 of Fig. 2]; a second communication path that coupled at least one pin of an embedded device to the test circuitry [I/O port 132 of

Fig. 2] and a third communication path that coupled an output of the test circuitry to an input of a fixed logic device [I/O_PIN 150 of Fig. 2].

25. As to claims 30-31, Shen teaches the test circuitry coupled to the FPGA to the embedded device whenever the FPGA configured to test the embedded device [see "interconnecting" of claim 2] and scan chain to the embedded device [col. 6 lines 45-57].

Allowable Subject Matter

26. Claim 19-21 and 32-33 are allowed.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2133